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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,189	09/17/1999	JUN KANAMORI	IIZ.008D	9755

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,189	KANAMORI, JUN	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6 and 24-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *2-6 and 24-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 CFR 114, claiming priority from parent case U.S. Serial No. 09/398,189 filed on September 17, 1999 which itself is divisional of U.S. Serial Number 09/342,751 filed on June 29, 1999 which papers have been placed of record in the file.

Request for Continued Prosecution Application (RCE)

The request filed on 01/13/2003 for a Request for Continued Prosecution Application (RCE) under 37 CFR 1.114 based on parent Application No. 09/398189 is acceptable and a RCE has been established. An action on the RCE follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed12 /10 / 2002 which has been entered on January 23, 2003.

Therefore claims 2-3, 24 and 30 as amended by the amendment and claims 31-34 presently newly recited and claims 4-6 and 26-29 as recited in the amendment filed on July 23, 2002 and entered on December 23, 2003 are currently pending in the application.

Drawings

The drawings filed on 09/11/1999 have been objected to for the reasons set out in the enclosed PTO-948.

The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-6 and 24 to 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPR (Applicants' Admitted Prior Art), Doan (U.S. Patent No. 5,946,595, herein after Doan) and Besser et al. (U.S. Patent No. 6,165,903, herein after Besser) and Xiang (U.S. Patent No. 6,015,752 , herein after Xiang) .

With respect to newly added claims 24 and 30, AAPR teaches the method of fabricating a semiconductor device including the steps of :

Providing a silicon substrate (AAPR fig. 1 # 12), providing a buried oxide layer on the silicon substrate (AAPR fig.1 # 14), providing a filed oxide layer and a silicon on insulator layer on the buried oxide layer (AAPR # 16 and 18) providing a gate oxide layer on the silicon on insulator layer (AAPR # 20), providing a metal layer (i.e. poly-silicon gate layer) on the gate oxide layer (AAPR # 22), providing a gate sidewall layer on the silicon on insulator layer to surround the poly-silicon gate layer and the gate

oxide layer (AAPR # 24), providing a material to be silicided on a surface of the semiconductor device including the poly silicon gate layer, the gate sidewall layer, the silicon on insulator layer and the field oxide layer (AAPR fig. 1B and C ultimately forming layer 32), performing a first rapid thermal annealing process to from first-reacted silicide regions in the poly-silicon gate layer and in source/drain active areas of the silicon on insulator layer (AAPR Applicants' specification –prior art section page 2 lines 9-14), removing non-reacted material from the first –reacted silicide regions (AAPR specification –prior art section page 2 lines 13-15).

AAPR does not specifically describe providing a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed.

However, Besser, a patent from the same filed of invention, describes in fig. 8 layer # 46 and col. 5 lines 25-40 to convert the first reacted silicide region into a second reacted silicide region and to prevent junction leakage problem.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Besser's second supplemental silicon layer in AAPR"s method steps to prevent junction leakage problem. (Besser col. 5 lines 65-col. 6 line 5).

AAPR and Besser do not specifically describe doping the supplemental silicon layer.

However, Doan, a patent from the same filed of endeavor, describes in fig. 8 and col. 6 lines 7-17 the doping of the supplemental silicon layer so that it can etched at a faster rate in comparison with the layers below it.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Doan's doping of the supplemental silicon layer step in AAPR , Besser's method to provide a doped layer that etches differently from the layers underlying it. (Doan col. 6 lines 31-37).

The supplemental silicon region preventing the poly-silicon gate layer and the silicon on insulator layer from being completely silicided (Doan col. 6 lines 36-39 and further as Doan and the instant application use the same materials in similar method steps for the same purpose what is true for applicants is also true for Doan).

"The semiconductor device including a p-channel MOS transistor having a p-type source and rain regions, and including an n-channel MOS transistor having n-type source and drains. "

AAPR, Besser and Doan do not specifically describe a CMOS device .

However, Xiang, col. 3 line 47, col.5 line 59-60 was cited to show that by definition (and as is well known to one of ordinary skill in the art) CMOS includes both n-channel transistor having n-type source and drain regions and p-channel transistors having p-type source and drain regions.

"Said doping comprising doping a p-type impurity into the supplemental silicon that is provided over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is provided over the n-channel Mos transistor. "

Further a p-type source/drain with a thin polysilicon strap (as shown in Doan i.e the supplemental silicon layer) would obviously have to be doped p-type to form an excellent ohmic contact and avoidance of a P-N diode formation and similarly for N-

type source/drain region the connecting strap (the thin poly silicon strap, i.e. supplemental silicon layer) would be doped N-type for the same reasons.

With respect to claims 2 and 3 wherein the material is cobalt or titanium (AAPR page 26 last two lines).

With respect to claim 4, wherein the polysilicon layer is formed by CVD (well known in the art).

With respect to claims 5 and 6 wherein the supplemental silicon layer is a _Si(amorphous silicon) formed by sputtering (Bresser col. 1 lines 34-36, col. 5 lines 35-40) and selectively removing non-reacted silicon from the second- reacted silicide region after the second rapid thermal annealing . (AAPR teaches a method of making a semiconductor device by a self aligned silicide process, including selectively removing non reacted silicon after RTA, the un reacted silicon will be removed during the wet etch and removing the un reacted silicon after first RTA as stated in the back ground art is not patentably distinct from removing it after second RTA).

Claims 25-29 repeat the steps of claims 2-6 above and are rejected for reasons stated under respective claims above.

Presently newly added claims 31-34 are rejected for the following reasons :

With respect to claims 31 to 34 , wherein the doping comprises of doping a p-type (n-type) impurity into the supplemental silicon layer so that only the supplemental silicon layer over the p-channel (n-channel) MOS transistor is doped p-type (n-type). (as shown in Doan i.e the supplemental silicon layer) would obviously have to be doped p-type to form an excellent ohmic contact and avoidance of a P-N diode formation and

similarly for N-type source/drain region the connecting strap (the thin poly silicon strap, i.e. supplemental silicon layer) would be doped N-type for the same reasons) .

Response to Arguments

Applicant's arguments filed 12/13/02 have been fully considered but they are not persuasive because the motivation to have p-type doped region for a p-channel MOS transistor as previously stated is to form an excellent ohmic contact but at the same time avoiding the formation of a p-n diode that would be formed if the p-channel MOS if doped with the only other possible ions namely n-type.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

March 18, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800